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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/824,389	04/02/2001	Jonathan Yang Chen	POU920000073US1	1894

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EXAMINER	
CHANDRASEKHAR, PRANAV	
ART UNIT	**PAPER NUMBER**
2115	4

DATE MAILED: 05/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

4

Office Action Summary	Application No.	Applicant(s)	
	09/824,389	CHEN, JONATHAN YANG	
	Examiner	Art Unit	
	Pranav Chandrasekhar	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2,3*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

In line 17 of page 5, the word "through" has been misspelled as "thorough".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al [US Pat No. 6,202,168] in view of Lo Galbo et al [US Pat No. 5,280,629].

Saito teaches

defining a delay detection and calibration phase [col. 7 lines 4-21. The comparison between the test patterns is made to detect delay. Based on the detected delay, calibrations are made in the form of increasing or decreasing delay in the variable delay circuit];

sending a predefined bus signal test pattern for each bus line during the delay detection and calibration phase [col. 7 lines 4-21; col. 3 lines 57-67. The arrangement of multiple logic circuits on the sender and receiver side are indicative of multiple bus lines for data transfer.];

using a predefined bus signal test pattern to determine a delay time for each bus line during the delay detection and calibration phase [col. 7 lines 4-21; col. 3 lines 57-67. The arrangement of multiple logic circuits on both the sender side and receiver side are an indication of there being a delay time detection on each bus line. The test pattern is viewed as being predefined based on the test pattern generator.];

adjusting a receiver for each bit line to receive incoming signals at a time based on the determination of the delay [col. 7 lines 4-21. The variable delay circuit is viewed as being an integral portion of the receiver.]; and

placing the bus system in a normal communication mode [col. 8 lines 9-19. The adjustment of delay on each line prior to normal transfer is an indication that the bus system is placed in a normal communication mode following the detection and calibration phase].

Saito does not explicitly teach the determination of a longest delay during the detection and calibration phase.

Lo Galbo teaches the determination of a longest delay [col.10 lines 5-9].

It would have been obvious to one skilled in the art to combine the teachings of Saito and Lo Galbo in order to account for delays along bus lines that are longer than the standard delays as taught by Saito and to prevent the skew of data signals transmitted over the bus lines due to a longest possible delay.

3. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al [US Pat No. 6,202,168] in view of Lo Galbo et al [US Pat No. 5,280,629] and further in view of Nagano [US Pat No. 6,335,647].

4. As per claim 2, Saito teaches circuitry to detect delay for each bit of a bus system [col. 7 lines 4-21; col. 3 lines 57-67. The plurality of logic circuits on both the sender side and receiver side are an indication of there being a delay time detection on each bus line].

Saito does not explicitly teach

worst case delay detection circuitry for each bit of the bus system; and

control circuitry coupled to the worst case delay detection circuitry for each bit; operative to select one of two receiver paths for each bit as a function of each bit's delay detection circuitry output and clock signals associated with each bit's receiver latch.

Lo Galbo teaches worst case delay detection circuitry for a single bus system [col. 10 lines 5-9];

Lo Galbo does not explicitly teach control circuitry coupled to the worst case delay detection circuitry for each bit; operative to select one of two receiver paths for each bit as a function of each bit's delay detection circuitry output and clock signals associated with each bit's receiver latch.

Nagano teaches

selecting one of several receiver paths for each bit as a function of each bit's delay with respect to a first bit [col. 5 lines 20-26; col. 5 lines 34-43; col. 5 lines 48-52].

Nagano does not explicitly teach selecting clock signals associated with each bit's receiver latch.

It would have been obvious to one skilled in the art to combine the teachings of Saito, Lo Galbo and Nagano to incorporate a worst case delay detection circuitry for each bit of the bus system and utilize the worst case delay as a parameter to select the receiver path for each bit since it would be advantageous to minimize the variations in propagation time of each bit. The different receiver paths are associated with varying degrees of delay. Thus, the appropriate amount of adjustment in delay may be selected on the basis of worst case delay detected for each channel. Furthermore, it would have been obvious to select clock signals associated with each bit's receiver latch.

5. As per claim 3, Saito, Lo Galbo and Nagano do not explicitly teach two of the bits having worst case delay detection circuitry adapted to use different clock phases of the synchronous bus system.

It would have been obvious to one skilled in the art to modify the teachings of Saito, Lo Galbo and Nagano to enable two of the bits to have worst case delay detection circuitry adapted to use different clock phases of the synchronous bus system.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pranav Chandrasekhar whose telephone number is 703-305-8647. The examiner can normally be reached on 8:30 a.m.-5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 703-305-9717. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Pranav Chandrasekhar
May 5,2004

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100